A D-LDD (Double Lightly-Doped Drain) STRUCTURE H-MESFET FOR MMIC APPLICATIONS

Yasuro Yamane, Kiyomitsu Onodera, Takumi Nittono, Kazumi Nishimura, Kimiyoshi Yamasaki and *Atsushi Kanda
NTT System Electronics Laboratories
and *NTT Wireless Systems Laboratories
3-1, Morinosato-Wakamiya, Astugi, Kanagawa, Japan, 243-01

ABSTRACT

This paper proposes a new D-LDD (Double Lightly-Doped Drain) structure for InGaP/InGaAs H-MESFETs (Heterostructure -MESFET) . A D-LDD H-MESFET has three kinds of low resistant layers in the drain region, while a conventional H-MESFET has two layers. This structure improves MAG accompanied by Rd reduction with minimized gate-breakdown-voltage degradation and Cgd increase. These trade-offs between Rd and breakdown voltage are discussed in detail. Consequently, a typical MAG at 50 GHz exhibits 8.9 dB S21 in a MESFET and 7.7 dB S21 in a 1-stage amplifier. The high-frequency circuit operation proves that this technology is one of the most promising for MMIC applications.

INTRODUCTION

In the coming multimedia age, ultra-broad-band wireless access systems will become necessary for dealing with large amounts of information. In order to realize these systems, microwave and millimeter-wave monolithic integrated circuits (MMIC) will be indispensable. In other words, a device, which has sufficiently high gain in the millimeter-wave region, must be developed for this new age.

For this purpose, p-HEMTs and InP-based HEMTs have been investigated for several years. However, these devices have a recessed gate structure to reduce parasitic resistance. Consequently, only one type of FET can be fabricated on a wafer, while integrating several different types would be attractive for highly functional integration of MMICs. In this paper, we will report the simultaneous fabrication of a 0.1 μm class symmetric LDD (Lightly Doped Drain) H-MESFET and a new structure, an asymmetric D-LDD (Double Lightly Doped Drain) H-MESFET, on the same wafer. An asymmetric D-LDD H-MESFET, has both high gain and high breakdown voltage, while a symmetric LDD H-MESFET has high current gain cut-off frequency (f_T).

DEVICE STRUCTURE

The new structure D-LDD H-MESFET is shown in Fig. 1. It has an i-InGaP barrier layer to improve breakdown voltage [1,2] and an n-InGaAs channel layer. InGaP is a very promising material for the barrier layer because it has no DX center, but it is difficult to form highly doped n-InGaP. Hence it is also difficult to attain a sufficiently high sheet carrier in the n-InGaP/GaAs or n-InGaP/InGaAs systems. With i-InGaP/n-InGaAs on the other hand, it is possible to obtain high sheet carrier [3,4].

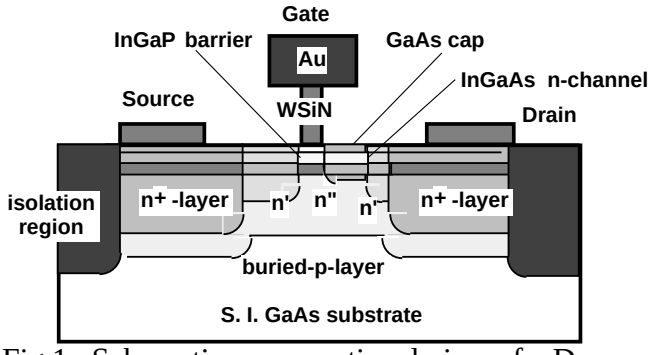


Fig.1. Schematic cross-sectional view of a D-LDD H-MESFET.

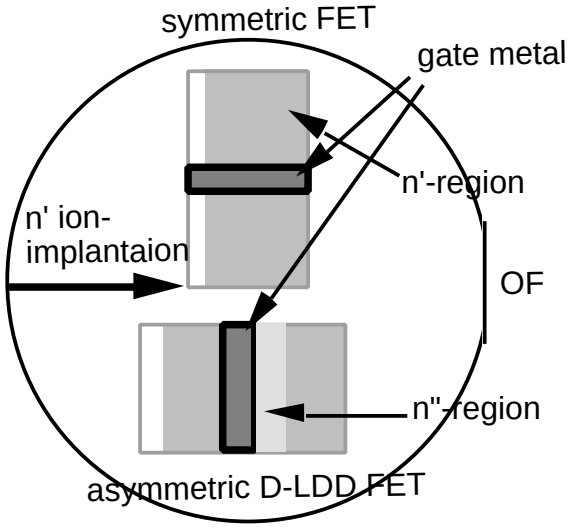
An FET with the D-LDD structure has two lightly-doped regions and one heavily-doped region only on the drain side, although there is

0-7803-4603-6/97/$5.00 (c) IEEE

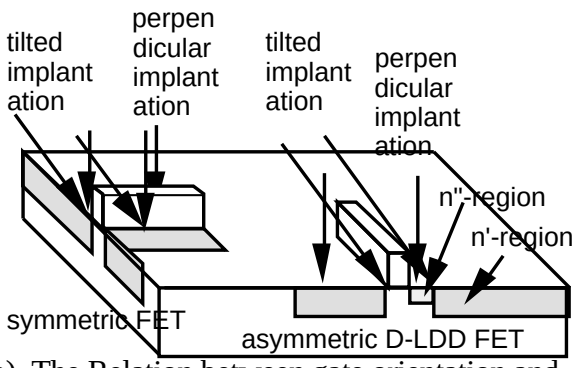
one lightly-doped region and one heavily-doped region on the source side. The lightly-doped region close to the gate is called the n"-layer, and the other lightly-doped layer is called the n'-layer. The n" implantation dose should be less than the n'-layer dose so as not to degrade the gate-drain breakdown voltage (Vbgd). We used an n" implantation dose ranging from 1/10 to 1/4 of the n' implantation dose.

FABRICATION PROCESS

The integration of D-LDD H-MESFETs and LDD H-MESFETs is easily achieved by changing the n' ion-implantation tilt angle [5,6], as shown in Fig. 2.



(a) Gate orientation of both types of FET in a wafer.



(b) The Relation between gate orientation and ion-implantation tilt-angle.

Fig. 2. Simultaneous fabrication of an asymmetric D-LDD H-MESFET and a symmetric LDD H-MESFET on the same wafer.

The gate orientations of a symmetric FET and an asymmetric FET are different as shown in Fig. 2 (a). An n' ion-implantation is achieved at a tilted angle from theinverse of OF (Orientation Flat). The region of shadow of gate metal is not implanted as shown in Fig. 2 (b). After tilted n'-implantation, the "-layer is implanted at a perpendicular angle. So, the region with no n'-implantation is implanted by n"-implantation. This procedure does not affect a symmetric FET's structure. Consequently, symmetric and asymmetric FETs can successfully fabricated on the same wafer.

THE ROLE OF Rd ON GAIN

The simple asymmetric structure reported in Refs. 2 and 3 has many advantages for other devices, but it has one problem: the drain resistance (Rd) can easily be affected by deviations in gate etching processing because there is a high resistive region with no implantation on the drain side as shown in Fig. 1. The D-LDD structure is proposed to overcome this drain resistance variation. Rd degrades gain at high frequency, shown in Fig. 3, which is the calculated result. This figure shows that Rd-Rs less than 100 Ω for a 10 μm Wg H-MESFET is necessary for millimeter-wave operation.

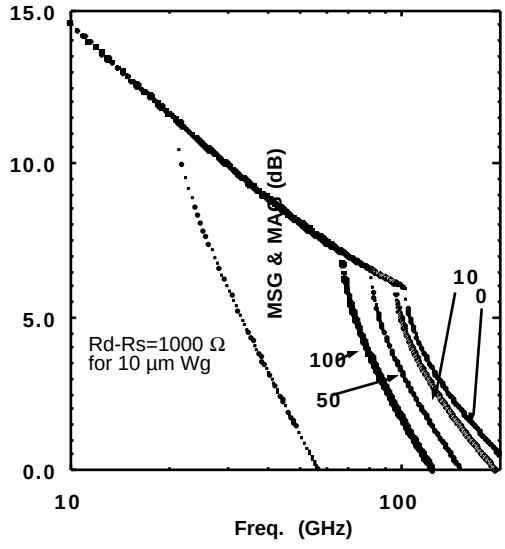


Fig. 3. Role of Rd on MSG and MAG frequency characteristics (calculated).

DEVICE CHARACTERISTICS TRADE-OFF RELATIONS

One probable problem caused by n" implantation is the decrease in gate breakdown voltage. The trade-off relations between Vbgd (gate-drain breakdown voltage) and Rd are shown in Fig. 4 as a function of the n" ion-implantation dose. Both Vbgd and Rd-Rs reduce with increasing n" dose. Rd-Rs becomes 0 Ω at $4x10^{13}$ cm^{-2}, because n'-dose is $4x10^{13}$ cm^{-2} and the FET becomes symmetric at this dose. Figure 4 shows that a Vbgd reduction of only 0.5 V allows a 100 Ω Rd reduction in a 10 μm Wg H-MESFET. Thus, $1x10^{13}$ cm^{-2} n" implantation is effective in Rd reduction with the trade-off that Vbgd only decreases by 0.5 V. Another likely problem is the increase in the Cgd. Figure 4 is the Cgd dependence on n"-implantation dose.

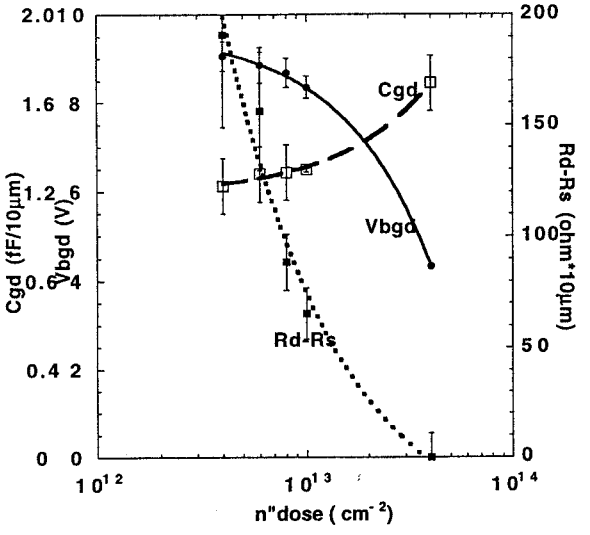


Fig. 4. Dependence of the gate-drain breakdown voltage, Rd and Cgd on n"-layer dose

The doses of n"-implantation are $4x10^{12}$, $6x10^{12}$, $8x10^{12}$ and $1x10^{13}$ cm-2. The Cgd increase under these conditions is only 0.1-0.2 fF /10 μm.

A 0.10 μm D-LDD H-MESFET with n"-implantation of 1 x 10^{13} cm^{-2} exhibited high MAG which is not inferior to a symmetric LDD H-MESFET as shown in Fig. 5. The measured MAG at 50 GHz and f_T was as high as 8.9 dB and 66.5GHz. The symmetric H-MESFET exhibits 8.2 dB and 72.1 GHz on the same wafer.

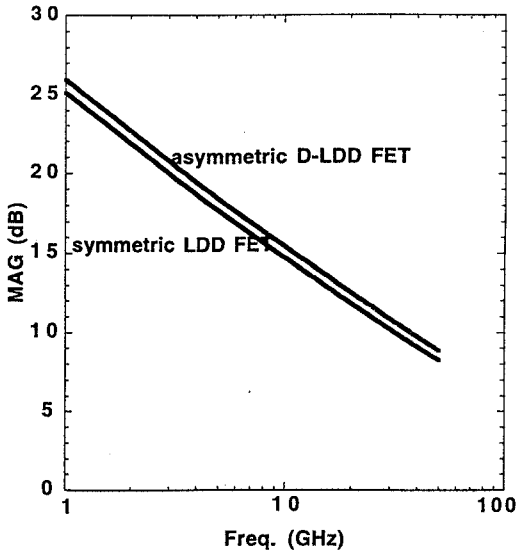


Fig. 5. MSG and MAG frequency characteristics of an asymmetric D-LDD H-MESFET and a symmetric LDD H-MESFET on the same wafer .

A 1-STAGE AMPLIFIER PERFORMANCE

As a benchmark for high-frequency operation, a 1-stage amplifier of symmetric H-MESFETs was fabricated. Figure 6 shows its measured S-parameters. The maximum measured S21 was 8.8 dB at 47.3 GHz. Additionally, all 8 measured circuits typically exhibited 7.7 dB S21 at 46.7-49.9 GHz. This high performance is superior to any reported for GaAs MMICs [7,8] and implies that this technology is most promising for MMIC applications.

CONCLUSIONS

A D-LDD structure for an asymmetric high-power H-MESFET was proposed to stabilize reduced Rd with minimizing Vb deterioration. This FET has been fabricated only by changing ion-implantation tilt angle and gate orientation. By optimizing the n"-layer condition, a D-LDD H-MESFET exhibits an over 8V breakdown voltage between the gate-drain and a high MAG of 8.9 dB at 50 GHz. Simultaneously, a symmetric LDD H-MESFET has also been

fabricated with higher f_T of 72 GHz on a same wafer. A 1-stage amplifier attained 8.8 dB gain at 47.3 GHz. This high performance shows the possibilities of this device in millimeter-wave applications.

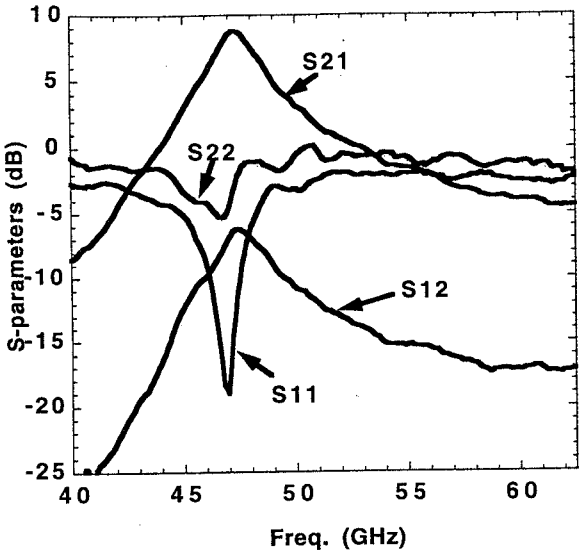


Fig. 6. Measured S-parameters of the 1-stage amplifier

ACKNOWLEDGMENTS

The authors would like to thank Drs. F. Hyuga, M. Hirano, M. Tokumitsu, H. Niiyama, S. Aoyama, K. Watanabe, S. Sugitani, M. Aikawa and M. Muragichi for their useful discussions.

REFERENCES

1. M. Razeghi et al., "$Ga_{0.5}In_{0.49}P/Ga_xIn_{1-x}As$ lattice-matched (x=1) and strained (x=0.85) two-dimensional electron gas field-effect transistors," Semicond. Sci. Technol. vol. 6, pp. 103-107, 1991
2. F. Hyuga et al. , "Si-implanted InGaP/GaAs metal-semiconductor field effect transistor," Appl. Phys. Lett. vol. 60, pp. 1963-1965, 1992
3. M. Takikawa et al., "Pseudomorphic n-InGaP/InGaAs/GaAs high electron mobility transistor for low-noise amplifier," IEEE Electron Device Lett., vol. 14, no. 8, pp.406-408, 1993
4. D. Geiger et al., "InGaP/InGaAs HFET with high current density and high cut-off frequencies," IEEE Electron Device Lett., vol. 16, pp. 259-261, 1995
5. S. Sugitani et al., "Self-aligned InGaP/InGaAs/GaAs heterostructure MESFET technology for analog-digital hybrid type ICs," 1994 GaAs IC Symposium Dig. pp. 123-136, 1994
6. K. Inoue et al., " Improvement of Breakdown Voltage in InGaP/InGaAs/GaAs Hetero structure MESFETs for MMICs," 1995 GaAs IC Symposium Dig., pp. 97-100, 1995
7. N. Camilleri et al. " Monolithic 40 to 60 GHz LNA," 1990 MTT-S Digest., pp. 599-602, 1990
8. C. L. Lau et al. "Millimeter wave Monolithic IC's using direct ion implantation into GaAs LEC substrate," 1990 GaAs IC Symposium Digest., pp. 73-77, 1990